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202-371-5950 2/2/2005 5:33 PAGE 001/005 Fax Server  
FROM: WINSTON & STRAWN LLP

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of: Eric NEYRET et al. Confirmation No.: 6832  
Application No.: 10/671,813 Group Art Unit: 2812  
Filing Date: September 25, 2003 Examiner:  
For: METHOD FOR MINIMIZING SLIP LINE Attorney Docket No.: 4717-7800  
FAULTS ON A SEMICONDUCTOR  
WAFER SURFACE

**REQUEST FOR CORRECTION OF FILING RECEIPT  
AND SUBMISSION OF SUPPLEMENTAL DECLARATION**

Office of Initial Patent Examination  
Filing Receipt Corrections  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

A Filing Receipt for the above-identified application has been received and the following correction is respectfully requested.


Please correct the filing date of the foreign priority application to 10/01/2002 (October 1, 2002). A copy of the Filing Receipt with the requested change noted thereon is attached.

Also enclosed is a Supplemental Declaration on which the filing date of the French priority application has been changed to "01 October 2002". This Supplemental Declaration also includes correction of the hand-written change made to the last name of inventor Ecartot.

No fee is believed to be due for this submission. Should any fees be required, however, please charge such fees to Winston & Strawn LLP Deposit Account No. 50-1814.

Respectfully submitted,

Feb. 2, 2005  
Date

  
E. Bradley Gould (Reg. No. 41,792)  
For: Allan A. Farucci (Reg. No. 30,256)

**WINSTON & STRAWN LLP**  
Customer No. 28765  
202-371-5771

DC:400037.1



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE RECD	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/671,813	09/25/2003	2812	880	4717-7800	2	19	3

28765  
WINSTON & STRAWN  
PATENT DEPARTMENT  
1400 L STREET, N.W.  
WASHINGTON, DC 20005-3502

CONFIRMATION NO. 8832

UPDATED FILING RECEIPT



\*0C00000011888230\*

Date Mailed: 02/25/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-8195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Eric Nayret, Sassenage, FRANCE;  
Christophe Maleville, La Terrasse, FRANCE;  
Ludovic Ecamot, Gleres, FRANCE;

Domestic Priority data as claimed by applicant

Foreign Applications

10/01/2002

FRANCE 0212120 01/10/2002

If Required, Foreign Filing License Granted: 12/16/2003

Projected Publication Date: 06/03/2004

Non-Publication Request: No

Early Publication Request: No

Title

Method for minimizing slip line faults on a semiconductor wafer surface

Preliminary Class  
438

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Title 35, United States Code, Section 184  
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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